

### REMARKS

Notice of non-compliance indicates that the newly added Claims 22-23 were inadvertently underlined. The Applicants have respectfully corrected the inadvertent underlining of the newly amended Claims 22-23. As such, Claims 22-23 are properly identified and therefore allowance of Claims 1-2, 4-10, 12 and 14-23 is earnestly solicited.

For Examiner's convenience, the Applicants have respectfully reproduced below, the Applicants' response mailed on December 5, 2006.

Claims 22 and 23 have been added without introducing new matter.

### Claim Rejections - 35 U.S.C. §102

Claims 1, 10 and 12 were rejected as being allegedly anticipated by U.S. Patent No. 5,371,878 (hereinafter "Coker"). Applicants respectfully traverse in view of the following.

Independent Claim 1 recites a limitation whereby a microcontroller executes a set of boot code and a virtual microcontroller execute a set of timing code wherein at least one portion of the set of timing code is different from the set of boot code, as claimed. Additionally, independent Claim 1 recites a limitation whereby at least one portion of the boot code is inaccessible to the virtual microcontroller, as claimed. Furthermore, independent Claim 1 recites a

limitation whereby the microcontroller and the virtual microcontroller halt simultaneously, as claimed.

In contrast, Coker discloses that a shadow system executes the same software as the target-ECS from system start-up or reset (see Coker, col. 2, lines 56-58). Moreover, Coker discloses that the shadow system and the target-ECS function exactly the same except that the shadow system receives data slightly delayed (see Coker, col. 2, lines 13-15). The rejection asserts that “the claim language does not exclude the virtual microcontroller from executing the same boot code as the microcontroller, but rather requires that the virtual microcontroller executes code timed to take the same number of clock cycles as the microcontroller uses to execute the boot code.” Accordingly, independent Claim 1 has been amended to further distinguish over Coker by reciting a limitation whereby at least one portion of the set of timing code is different from the set of boot code, as claimed.

With regard to the limitation whereby at least one portion of the boot code is inaccessible to the virtual microcontroller, as claimed the rejection asserts that “Interface means 19 connecting the target-ECS and shadow system is used by Coker to transmit I/O data and does not appear to contain any suggestion that instruction code or boot code is transmitted via interface means (see column 4, lines 9-18).” Additionally the rejection directs the Applicants’ attention to Coker, FIG 1, which “depicts a one way flow of data from the target-ECS to the shadow system, denoted by arrows 18 and 26.” The rejection further asserts that “Coker

discloses a system wherein I/O data is transmitted from the target-ECS to the shadow system” and further asserts that “Coker in no way discloses that the shadow system accesses the target-ECS.” The Applicants respectfully disagree for the following reasons.

Coker discloses that the shadow system receives its input data from the input registers of the target-ECS (see Coker, col. 2, lines 61-62) and uses the data value and relative time of input events from the target-ECS (see Coker, col. 2, lines 65-67). Moreover, Coker discloses that the shadow system and the target-ECS function exactly the same except that the shadow system receives data slightly delayed (see Coker, col. 3, lines 13-15). In order to function exactly the same, the shadow system must necessarily have access to the same software. In fact, Coker itself discloses that a shadow system of this invention executes the same software as the target-ECS from system start-up (see Coker, col. 2, lines 56-57). Accordingly, Coker specifically teaches that the shadow system and the target-ECS function exactly the same by virtue of executing the same software. As such, Coker teaches that the same software is accessible to both the shadow system and the target-ECS and that they both execute the same software. Accordingly, Coker not only fails to teach that at least portion of the boot code is inaccessible to the virtual microcontroller, as claimed but it teaches away by teaching that the same software is executed by the shadow system and the target-ECS. Therefore, the Examiner is misguided in asserting that “there is no evidence whatsoever in the prior art reference that the boot code stored on the target-ECS is accessible to the shadow system.”

Moreover, Coker discloses that the execution states of the shadow system will lag slightly behind that of the target-ECS because of the slight time delay but the time when any given instruction is executed will directly correspond to the execution state of the target-ECS when the same instruction was executed (see Coker, col. 8, lines 41-49). By definition, if the shadow system lags behind the target-ECS, then they cannot halt simultaneously, as claimed.

Moreover, the rejection asserts that it is inherent that a computer process in a debugger system halts because there is a distinct conclusion to the debugging process. The Applicants disagree because it is possible to log the information for debugging purposes and analyzing the logged information at a later time. Therefore, it is not inherent that a computer process in a debugger system halts as suggested by the rejection. As such, Coker fails to teach or suggest simultaneously halting the microcontroller and the virtual microcontroller, as claimed.

Accordingly, Coker fails to teach or suggest the recited limitations of independent Claim 1. As such, independent Claim 1 is patentable over Coker, under 35 U.S.C. 102(b). Independent Claims 10 and 12 recite at the recited limitations of independent Claim 1 discussed above and are therefore patentable over Coker, under 35 U.S.C. 102(b), for similar reasons.

Moreover, regarding Claim 10, the rejection asserts that removing the break, as claimed is regarded as the necessary and inherent steps of practicing Coker's invention in order to debug the system. As discussed above, Coker fails to teach or suggest halting the microcontroller and the virtual microcontroller, as claimed. Accordingly, Coker also fails to teach or suggest removing the break, as claimed for similar rationale.

Moreover, "to establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.' " In re Robertson, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999). "In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." Ex parte Levy, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990). As such, the Applicants respectfully invite the Examiner to introduce extrinsic evidence to establish the alleged inherency if the rejection is to be maintained. Accordingly, independent Claim 10 is patentable over Coker.

As such, allowance of Claims 1, 10 and 12 is earnestly solicited.

Claim Rejections - 35 U.S.C. §103

Claims 1-2, 4-10, 12 and 14-20 were rejected as allegedly being unpatentable over U.S. Patent No. 6,202,044 (hereafter "Tzori"). Applicants respectfully traverse in view of the following.

Independent Claim 1 recites (emphasis added):

A boot method for an In-Circuit Emulation system having a microcontroller operating in lock-step synchronization with a virtual microcontroller, comprising:  
in the microcontroller, executing a set of boot code to substantially carry out initialization;

in the virtual microcontroller, executing a set of timing code to enable the lock-step synchronization, wherein the timing code is timed to take the same number of clock cycles as the microcontroller uses to execute the boot code, and wherein at least one portion of said set of timing code is different from said set of boot code, and wherein the boot code is stored within the microcontroller and at least one portion of the boot code is inaccessible to the virtual microcontroller;  
and

simultaneously halting both the microcontroller and the virtual microcontroller.

Booting is a process that starts a system (e.g., operating system) and substantially initialize the system when a user turns on a computing system or a system with a processor. Accordingly, booting takes place before actual processing (e.g., simulation) by the system can take place.

Tzori discloses that the configuration data is loaded into the configurable-logic ICs (see Tzori, col. 7, lines 66-67 and see Figure 2 element 118) such that bit-slice data stream can be downloaded to the configurable-logic ICs during the stimulation-response cycle (see Tzori, col. 8, lines 18-24). Tzori further discloses that during the initialization interval logic-configuration data is loaded into the configurable-logic ICs, after which the simulation process performs a sequence

of simulation cycle (see Tzori, col. 9, lines 20-30). The rejection admits that “the rejection is based upon the method disclosed by Tzori that occurs after the initialization process.” Accordingly, Claim 1 is distinguishable over Tzori by reciting a limitation whereby a microcontroller executes a set of boot code to substantially carry out initialization, as claimed.

The cited reference fails to teach or suggest a virtual microcontroller executing a set of timing code, as claimed because as admitted the rejection is based upon the method disclosed by Tzori that occurs after the initialization process. Similarly, Tzori fails to teach or suggest that the timing code is timed to take the same number of clock cycles as the microcontroller uses to execute the boot code, as claimed for the same rationale discussed above. Moreover, Tzori fails to teach or suggest that at least one portion of said set of timing code is different from said set of boot code, as claimed for similar rationale discussed above. Furthermore, Tzori fails to teach or suggest that the boot code is stored within the microcontroller and at least one portion of the boot code is inaccessible to the virtual microcontroller, as claimed for rationale similar to that discussed above.

Moreover, Tzori fails to teach or suggest executing a set of timing code to enable lock-step synchronization, as claimed. In fact, Tzori teaches away from operating in lock-step synchronization by disclosing that an object of the invention disclosed in Tzori is to provide a digital logic simulation/emulation system that may be freed from lock-step synchronization between the simulation

computer program and the digital logic circuit's stimulation response cycles (see Tzori, col. 4, lines 50-55).

The rejection without providing any support asserts that the step of simultaneously halting is well known in the art as a breakpoint for a concurrent process. The rejection further asserts that Tzori's system and method are clearly conducive to this type of breakpoint, achieved by using the control data during the engaged mode to simultaneously halt both the microcontroller and virtual microcontroller. The Applicants respectfully disagree because as discussed above and as admitted by the rejection the rejection is based upon "the method disclosed by Tzori that occurs after the initialization process." Accordingly, what Tzori may be conducive to is irrelevant since the claimed invention is directed to a boot method, as claimed which is not after the initialization process as discussed above.

Moreover, the Applicants respectfully remind the Examiner that to establish a *prima facie* case of obviousness, the prior art reference (or references when combined) must teach or suggest all the claim limitations (see MPEP 2100-126). Accordingly, the Applicants respectfully submit that it is improper for the Examiner without any evidentiary support to rely on his common knowledge to reject the claimed limitation. As such, an affidavit or evidentiary support for the assertion is requested should the rejection be maintained.

Additionally, the rejection states that “it appears that the Applicants’ claimed invention inherently initializes a programmable logic device, as does Tzori” and requests clarification. The Applicants respectfully assert that the newly amended Claim 1 further clarifies the claim. Claim 1 recites a microcontroller executing a set of boot code to substantially carry out initialization, as claimed and a virtual microcontroller executes a set of timing code, as claimed. Accordingly, the virtual microcontroller executes a set of timing code, as claimed.

Accordingly, Tzori fails to teach or suggest the recited limitations of independent Claim 1. As such, Tzori fails to render independent Claim 1 obvious, under 35 U.S.C. 103. Independent Claims 10 and 12 also recite limitations similar to that of independent Claim 1 discussed above. As such, Claims 10 and 12 are patentable over Tzori for reasons similar to that of independent Claim 1. Dependent claims are patentable by virtue of their dependency.

Moreover, regarding Claims 7 and 18 Official Notice was taken that breakpoints are well known in the art and in support of the Official Notice the rejection points the Applicants to page 3, lines 1-7. The Applicants respectfully assert that knowledge of breakpoints does not teach or suggest that prior to the executing of the boot code, and prior to executing the timing code, setting a break at an assembly instruction line, as claimed. Moreover, the mere knowledge that a breakpoint may be used does not teach or suggest that after executing of the boot code and the timing code, the microcontroller and the virtual

microcontroller branch to the assembly instruction line respectively, as claimed. In other words, the mere fact that a breakpoint may be used does not necessitate setting it at a given assembly instruction line, executing boot code and timing code and then branching to the assembly instruction line, as claimed. Therefore, Official Notice taken by the Examiner is improper. As such, proper evidentiary support or an affidavit is kindly requested should the rejection based on the Official Notice be maintained.

Moreover, regarding Claims 9 and 20 the rejection takes Official Notice that “removing breakpoint is well known in the art” and directs the Applicants to page 3, lines 1-7 of the Application. Similar to the rationale presented above, knowledge that a breakpoint may be used does not necessarily teach or suggest removing the break after copying the register contents and copying the memory contents, as claimed. Therefore, Official Notice taken by the Examiner is improper. As such, proper evidentiary support or an affidavit is kindly requested should the rejection based on the Official Notice be maintained.

The rejection asserts that “the ubiquity of commercial computer software, ostensibly having being debugged using breakpoints, which executes on the end-user’s computer without halting for the far-away programmer to examine the behavior of the program, is evidentiary support that it is well known to remove a breakpoint from computer code for at least the reasons of commercial deployment” and further states that “any allegation to the contrary is simply

unreasonable." The Applicants respectfully disagree with the Examiner's assertion for the reasons described above.

Moreover, the Applicants note that the rejection uses inherency and Official Notice for at least nine rejections. The remaining claims were rejected based on the combination of limitations found in claims already rejected. The Applicants would like to remind the Examiner that in limited circumstances, it is appropriate for an examiner to take official notice, however such rejections should be judiciously applied (see MPEP 2100-133) and while Official Notice may be relied on, these circumstance should be rare when an application is under final rejection or action under 37 CFR 1.113 (see MPEP 2100-134). The Applicants respectfully submit that taking Official Notice and inherency for almost half of the claims is contrary to judicious application.

Moreover, Official Notice unsupported by documentary evidence should be only be taken by examiner where the facts asserted to be well-known, or to be common knowledge in the art are capable of instant and unquestionable demonstration as being well-known (see *In re Ahlert*, 424 F.2d 1088, 1091, 165 USPQ 418, 420 (CCPA 1970)). The Applicants respectfully remind the Examiner that the Examiner has not met his burden for documentary evidence for taking Official Notice for the reasons described above.

As such, allowance of Claims 1-2, 4-10, 12, 14-20 and 22-23 is earnestly solicited.

Claim 21 was rejected as being allegedly unpatentable by Tzori in view of "Emulation of the Sparcle Microprocessor with the MIT Virtual Wires Emulation System" by Matthew Dahl et al. (hereinafter "Dahl") and in further view of "A Reconfigurable Logic Machine for Fast Event-Driven Simulation" by Jerry Bauer et al. (hereinafter "Bauer"). Applicants respectfully traverse because dependent Claim 21 is patentable by virtue of its dependency from the independent Claim 12. The Applicants do not understand either Dahl or Bauer to remedy the failures of Tzori as discussed above. As such, Tzori alone or in combination with Dahl and Bauer does not render Claim 21 obvious, under 35 U.S.C. §103(a). As such, allowance of Claim 21 is earnestly solicited.

For the above reasons, the Applicants request reconsideration and withdrawal of the rejections under 35 U.S.C. §102 and 35 U.S.C. §103.


### CONCLUSION

In light of the above listed remarks, reconsideration of the rejected Claims is requested. Based on the arguments presented above, it is respectfully submitted that Claims 1-2, 4-10, 12 and 14-23 overcome the rejections of record and, therefore, allowance of Claims 1-2, 4-10, 12 and 14-23 is earnestly solicited.

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